

THAT WHICH IS CLAIMED IS:

1. A vertical-conduction and planar-structure MOS device having a double thickness of gate oxide characterised in that it comprises:

- a first portion (5a) of gate oxide having a lower thickness in a channel area close to the active areas (4), and a second portion (5b) of thicker gate oxide in a central area (11) on a JFET area and
- an enrichment region (9) in said JFET area under said second portion (5b) of thicker gate oxide (11).

2. A MOS device according to claim 1, characterised in that said enrichment region (9) is self-aligned with said second portion (5b) of thicker gate oxide.

3. A MOS device according to claim 1, characterised in that said double thickness of gate oxide globally has a reduced surface reducing the distance between adjacent body wells enveloping said active areas (4).

4. A MOS device according to claim 1, characterised in that it comprises a polysilicon layer (13) on said first portion (5a) of thin gate oxide.

5. A MOS device according any of the previous claims, characterised in that it comprises respective first portions (5a) of thin gate oxide at the periphery of said second portion (5b) of thicker gate oxide.

6. A method for realising on a semiconductor substrate (2) MOS transistor (1) electronic devices with improved static and dynamic performances and high scaling down density, said transistors having traditional active areas (4) defined in the substrate (2) at the periphery of a channel region whereon a gate region is realised, characterised in that it comprises at least the steps of:

- realising the MOS transistor starting from a planar structure with a double thickness of gate oxide comprising a thin layer in the channel area close to the active areas (4) and a thicker layer in the central area (11) on the channel; and

- realising an enrichment region (9) in the JFET area below said thicker layer.

7. A method according to claim 6, characterised in that said enrichment region (9) is realised in parallel and in a self-aligned way with said thicker oxide layer.

8. A method according to claim 6, characterised in that said double thickness of gate oxide globally has a reduced surface reducing the distance between adjacent body wells enveloping said active areas (4).

9. A method according to claim 6, characterised in that, after defining the active areas (4) at the periphery of the channel region, it comprises the following operating steps:

- growing a pad oxide (5) on the active

areas (4) and on the channel for a thickness of about 100-500 Å;

- depositing a nitride layer (6) of 300-900 Å on the oxide layer (5);

- photomasking to define the inactive areas (11) which must have a thicker oxide layer;

- etching the nitride layer (6) removing the same on the channel up to expose the oxide layer (5);

- further implanting to realise said enrichment region (9) in the channel central area using the photoresist as implant window;

- removing the photoresist and growing said first thicker gate oxide layer (8);

- etching the nitride layer (6);

- selectively etching to remove also the oxide layer (5) on the active areas (4);

- growing a sacrificial oxide layer;

- wet etching this sacrificial oxide layer to expose the gate region of the transistor (1) on the channel;

- growing a second gate oxide layer at the periphery of the thicker oxide area (11).

10. A method according to claim 9, characterised in that said implant step is performed with P, As or Sb ions for a N-channel transistor and B or Al ions for a P-channel transistor, the implant energy is regulated between 60-900 KeV while ion doses can range from $1E12$ and $1E13$ ions/cm².

11. A method according to claim 6, characterised in that, after defining the active areas

(4) at the periphery of the channel region, comprises the following operating steps:

- growing the gate oxide on the active areas (4) and on the channel for the thickness required for the device correct operation (100-1500 Å);
- depositing a polysilicon layer (13) having a thickness being lower or equal to half the thickness of the thicker gate oxide part;
- depositing a nitride layer (6) of 300-900 Å on the polysilicon layer (13);
- photomasking to define the inactive areas (11) which must have a thicker oxide layer;
- etching the nitride layer (6) removing the same on the channel up to expose the polysilicon layer (13);
- further implanting to realise said enrichment region (9) in the channel central area using the photoresist as implant window;
- removing the photoresist and completely oxidising the polysilicon (13) not covered by the nitride layer (6);
- etching the nitride layer (6);
- depositing a conductive layer (12) to realise the gate electrode.

12. A method according to claim 11, characterised in that said implant step is performed with P, As or Sb ions for a N-channel transistor and B or Al ions for a P-channel transistor, the implant energy is regulated between 60-900 KeV while ion doses can range from $1E12$ and $1E13$ ions/cm².

13. A method according to claim 11,

characterised in that said conductive layer (12) to realise the gate electrode is composed of conveniently doped polysilicon.

14. A method according to claim 11, characterised in that said conductive layer (12) to realise the gate electrode is composed of a metal layer.